AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) The solid state energy converter of claim 17 [[1]], further comprising a collector region in thermal communication with a cold heat exchange surface, the collector region being in electrical and thermal communication with the gap region.

3. (Previously Presented) The solid state energy converter of claim 2, wherein the gap region is adjacent to the collector region.

4. (Original) The solid state energy converter of claim 2, further comprising a first ohmic contact in electrical communication with the emitter region.

5. (Original) The solid state energy converter of claim 4, further comprising a second ohmic contact in electrical communication with the collector region.

6. (Original) The solid state energy converter of claim 5, wherein the first and second ohmic contacts close an electrical circuit through an external load for heat to electricity conversion.

7. (Original) The solid state energy converter of claim 5, wherein the first and second ohmic contacts close an electrical circuit through an external power source for electricity to refrigeration conversion.

8. (Currently Amended) The solid state energy converter of claim 17 [[1]], wherein the emitter region comprises a metal or a highly doped semiconductor.

9-11. (Cancelled)

12. (Original) The solid state energy converter of claim 17 [[1]], wherein the p^* doping concentration of the p-type barrier layer relates to the n doping concentration of the gap region as $p_i > n_i (m^*_p / m^*_n)$, where m^*_p is the effective mass of holes, m^*_n is the effective mass of electrons, and subscript i denotes ionized fraction of carriers at a given temperature.

13. (Original) The solid state energy converter of claim 2, wherein the collector region comprises an additional injection barrier layer with a carrier concentration p^{**} that is adjacent to the gap region to reduce a thermoelectric back flow component.

14. (Previously Presented) The solid state energy converter of claim 2, wherein the collector region comprises an additional compensation layer with acceptor concentration p^* serving as a blocking layer at a cold side of the converter, and the acceptor concentration p^* being the same as the donor concentration in the gap region.

15. (Previously Presented) The solid state energy converter of claim 2, wherein the collector region comprises two p-type layers, one layer with a carrier concentration p^* serving as a blocking layer at a cold side of the converter, and the other layer with a carrier concentration p^{**} serving as an additional injection barrier layer and being adjacent to the gap region to reduce a thermoelectric back flow component.

16. (Original) The solid state energy converter of claim 13, wherein the p^{**} doping concentration of the additional injection barrier layer relates to the n doping concentration of the gap region as $p_i > n_i (m^*_p / m^*_n)$, where m^*_p is the effective mass of holes, m^*_n is the effective mass of electrons, and subscript i denotes ionized fraction of carriers at a given temperature.

17. (Original) A solid state energy converter with *n*-type conductivity, comprising:

an emitter region in thermal communication with a hot heat exchange surface, the emitter region comprising an *n*-type region with donor concentration n^* for electron emission;

a *p*-type barrier layer with acceptor concentration p^* adjacent to the emitter region, the *p*-type barrier layer configured to provide a potential barrier and Fermi-level discontinuity; and

a segmented gap region adjacent to the *p*-type barrier layer and comprising a first layer of a semiconductor material, and a second layer of a metal or a different highly *n*-doped semiconductor material, the second layer reducing heat flow density.

18. (Original) The solid state energy converter of claim 17, further comprising a first ohmic contact in electrical communication with the emitter region.

19. (Original) The solid state energy converter of claim 17, further comprising a second ohmic contact in electrical communication with the gap region.

20. (Original) The solid state energy converter of claim 17, wherein the first layer is at least 1 electron scattering length wide.

21. (Original) The solid state energy converter of claim 17, wherein the first layer is at least 5 electron scattering lengths wide.

22. (Currently Amended) A solid state energy converter with *p*-type conductivity, comprising:

an emitter region in thermal communication with a hot heat exchange surface, the emitter region comprising a *p*-type region with acceptor concentration p^* for hole emission;

a semiconductor gap region with an acceptor doping *p*, the gap region in electrical and thermal communication with the emitter region, wherein the gap region is segmented and comprises a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material; and

an *n*-type barrier layer with donor concentration n^* interposed between the emitter region and the gap region, the *n*-type barrier layer configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region.

23. (Previously Presented) The solid state energy converter of claim 22, further comprising a collector region in thermal communication with a cold heat exchange surface, the collector region being in electrical and thermal communication with the gap region.

24. (Previously Presented) The solid state energy converter of claim 23, wherein the gap region is adjacent to the collector region.

25. (Original) The solid state energy converter of claim 23, further comprising a first ohmic contact in electrical communication with the emitter region.

26. (Original) The solid state energy converter of claim 25, further comprising a second ohmic contact in electrical communication with the collector region.

27. (Original) The solid state energy converter of claim 26, wherein the first and second ohmic contacts close an electrical circuit through an external load for heat to electricity conversion.

28. (Original) The solid state energy converter of claim 26, wherein the first and second ohmic contacts close an electrical circuit through an external power source for electricity to refrigeration conversion.

29. (Original) The solid state energy converter of claim 22, wherein the gap region is at least 1 carrier scattering length wide

30. (Original) The solid state energy converter of claim 22, wherein the gap region is at least 5 carrier scattering lengths wide.

31. (Currently Amended) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n$ on a hot side of the converter, the n^* representing a n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, and the n representing a n-type segmented gap region with a donor concentration n and comprising a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

32. (Currently Amended) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n/p_c$ on a hot side of the converter, the n^* representing a n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, the n representing a segmented n-type gap region with a donor concentration n and comprising a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material, and the p_c representing a p-type compensation layer acting as a collector blocking barrier with acceptor concentration p^*, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

33. (Currently Amended) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n/p_i$ on a hot side of the converter, the n^* representing a n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, the n representing a segmented n-type gap region with a donor concentration n and comprising a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material, and the p_i representing an additional p-type barrier region with an acceptor concentration p^{**}, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

34. (Previously Presented) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $n^*/p/n/p_i/p_c$ on a hot side of the converter, the n^* representing a n-type emitter region with a donor concentration n^*, the p representing a p-type barrier region with an acceptor concentration p, the n representing a n-type gap region with a donor concentration n, the p_i representing an additional p-type barrier region with a donor concentration p^{**}, and the p_c representing a p-type compensation layer acting as a collector blocking barrier with a donor concentration of p^*, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with an n^* layer.

35. (Currently Amended) A method for converting thermal energy to electric energy, or electric energy to refrigeration, comprising:

injecting carriers into an *n*-type gap region from a highly doped *n** emitter region through a *p*-type barrier layer positioned between the emitter region and the gap region, wherein:

the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

the gap region is segmented and comprises a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material;

allowing for discontinuity of corresponding Fermi-levels; and

forming a potential barrier to sort electrons by energy.

36. (Currently Amended) A method for converting thermal energy to electric energy, or electric energy to refrigeration, comprising:

injecting carriers into a *p*-type gap region from a highly doped *p** emitter region through an *n*-type barrier layer positioned between the emitter region and the gap region, wherein:

the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

the gap region is segmented and comprises a first layer of a semiconductor material and a second layer of a metal or a different semiconductor material;

allowing for discontinuity of corresponding Fermi-levels; and

forming a potential barrier to sort electrons by energy.

37. (New) A solid state energy converter, comprising:

a thermal diode stack comprising:

a first diode with a design structure of $p^*/n/p/n_i/n_c$ on a hot side of the converter, the p^* representing a p-type emitter region with an acceptor concentration p^*, the n representing a n-type barrier region with a donor concentration n, the p representing a p-type gap region with an acceptor concentration p, the n_i representing an additional n-type barrier region with a donor concentration n^{**}, and the n_c representing a n-type compensation layer acting as a collector blocking barrier with a donor concentration of n^*, wherein the barrier layer is configured to provide a potential barrier and Fermi-level discontinuity between the emitter region and the gap region; and

a plurality of diodes having the same structure as the first diode that terminate on a cold side of the converter with a p^* layer.